Comparative Analysis of the Number of Mounting Elements and Wire Layers of an Integrated Circuit and a Printed Circuit Board Design

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***Abstract*— The fair compromise method is proposed, by which the number of the wire layers and elements of the mounting field of the IC and MPC are determined. A system of programs in the algorithmic language C++ and the application program Wolfram-Mathematica has been developed, which allows, at an early stage of design, to automatically determine the best ratio of the number of wire layers and elements of the mounting field of the IC and MPC platform by the minimum area of the mounting field and the maximum fill factor.**

***Keywords*— Integrated circuit, platform, mounting field, number of wire layers.**

I. INTRODUCTION

At the early stages of designing the structure of an integrated circuit (IC) and multilayer printed circuit boards (MPC), when we have no idea about the design yet, approximate methods are needed to estimate the average number of wire layers of the mounting field of the IC and MPC platform being designed [1-6]. As expected, at first, the preliminary methods were aimed at checking the design solutions of this or that structure from the standpoint of physical implementation.

In general, the development of methods of preliminary assessment for designing the structure was necessary primarily to reduce the time of the equipment development based on the ever-increasing high requirements set for technical parameters.

The main objective of this work, within the framework of automated design systems, is to determine the best ratio between the number of wire layers and the elements of the mounting field of an integrated circuit and the printed circuit board, which ensures the maximum filling and minimum surface values of the mounting field.

II. THEORY

Using the mathematical model [7,8], the number of wire layers on the mounting field of the IC and MPC platform was determined:

$$\gamma = \frac{\sum S_{met}}{K \cdot S} = \frac{d_{min}\bar{L}}{KabN} = \frac{tm_0 d_{min}(1-p)(N+N^P)N^{0.5(p-1)}}{K\sqrt{ab}(1+p)(N^{0.5}-N^{0.5p})}, \quad (1)$$

where γ is the number of wire layers of the mounting field of the IC and MPC platform; $\sum S_{met} = d_{min}\bar{L}$- the total area of the lengths of the wires of the electrical connections; K- the density coefficient of the wires of the wire layer; S - the whole surface of the mounting field platform; d_{min}- the wire width; $\bar{L}$- the sum of the lengths of the wires of the electrical connections of the IC and MPC mounting field platform; $a \times b$ - the distance between the elements in the horizontal and vertical directions, respectively; N - the number of elements in IC; t- the branching coefficient of the circuits $(0{,}5 \le t < 1)$; $m_0 -$ the average number of outputs of the elements; $p -$ the density coefficient of the inter-element connections $(0{,}1 \le p \le 1)$.

The dependence (1) allows for solving a several of synthesis problems.

Let's consider $\gamma = f(N)$, when the curve system $K = const$, $\gamma = f(k)$, when $N = const$, $S = f(N)$, when $\gamma = const$ and $s = f(\gamma)$, when $N = const$ (Fig 1.2). The obtained curves of constancy $\gamma = f(N)$ and $s = f(N)$ coincide with the results of the works [7-8]. It is known that different surfaces have different mounting characteristics. Using these dependencies, it is possible to study the dependence of the same degree of integration N of the IC and MPC platforms on surfaces and wire layers (Fig. 2).

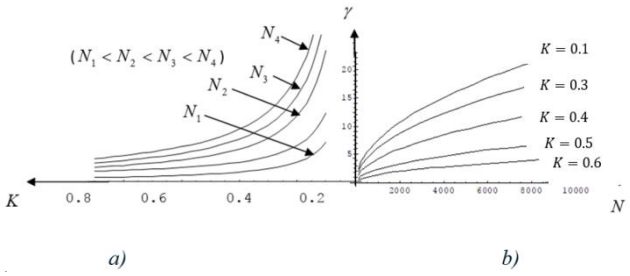

Fig. 1. The dependence of the number of the wire layers of the integrated circuit platform on the wire density coefficient K of the mounting field (a) and the number of elements N of the integrated circuit (b)

The private problems of the studied synthesis are scalar by nature. According to the selected indicators, when setting up the vector problem of synthesizing structures, we should take

into account that the solution of such a multi-criteria problem cannot be the only one for all cases of the IC and MPC design.

Only the technical specification of the design defines the structural requirements, according to which it is possible to formulate the synthesis problem as a vector one and choose a way for its solution. It should be noted that at the synthesis of the IC and MPC structures according to some indices, it is expedient to use the multicriteria optimization methods by giving a geometrical explanation to the solution. This expediency is conditioned primarily by the facts that the constancy curves constructed on the obtained expressions are quite visual and show the possible solutions in the permissible solution range (PSR) [8,9].

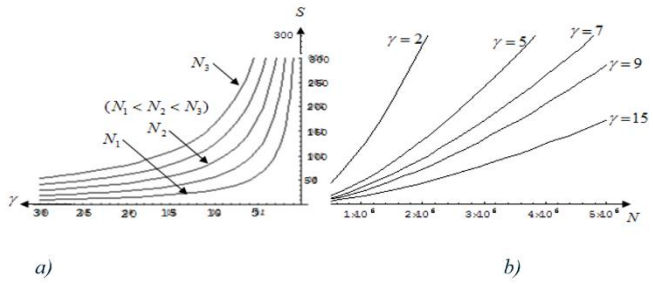

Fig. 2. The dependence of the IC platform surface S on the number of the wire layers and the number of elements N of the mounting field

The constancy curves (Fig. 1, 2) are the basis on which, according to the IC and MPC platform, the number of wire layers and the solution of the vector synthesis problem of the parameter structures of the number of elements are based [8,9].

The solutions are determined in a two-dimensional Cartesian coordinate system, where the number of wire layers of the integrated circuit γ is placed on the ordinate axis, and the number of N elements on the abscissa axis. To illustrate the methodology of using the constancy curves in solving vector synthesis problems, let's consider an example [8,9].

Let's assume that it is required to solve the synthesis problem of the IC and MPC structure according to two criteria:

1. The minimum area of the mounting field of the IC and MPC platform;
2. The maximum K of the density coefficient of the wires of the mounting field wire layer of the IC and MPC platform.

The first is one of the main design criteria, and the second is determined by the requirement of the shrinkage of the unused surfaces on the platform, which leads to the reduction of the unnecessary mounting field. The initial data to solve the synthesis problem are: the schematic diagram of the IC and MPC; the limitations of the mounting field $S, K, N,$ and γ parameters of the integrated circuit platform; the limitations of the selected indicators; the requirement for constructing a structure on one integrated circuit type-size, i.e., the area of the mounting field of its platform at the specified geometric dimensions of the integrated circuit.

If there is no limitation on the minimum geometric dimensions of IC and MPC, in particular on the surface, then their limitations can be determined when solving the problem.

As it is known, the reduction in the overall dimensions of IC and MPC is limited from bottom by the requirement to ensure the thermal regime and the number of wire layers γ in the mounting field of the platform.

The solution of the problem is based on γ and N indicators in the presence of S_{min} and K_{max} limitations. First of all, to solve the problem, it is necessary to define the range of permissible solutions (PSR). The limitations of the IC γ and N parameters establish (determine) a certain range of permissible solutions, within which it is necessary to determine the optimal values of the $N, S, K,$ and parameters. That range is the ABCD rectangle (Pareto range) [8,9].

PSR is limited by the surface $S_{min}(\gamma, N)$ of the IC platform and the density coefficient $K_{max}(\gamma, N)$ of the wire layers of the mounting field platform in the field $\gamma(N)$ (Fig.3).

The number of wire layers of the IC platform is limited by the maximum γ_{max} value on top - the number of wire layers of the platform from the available list and from the bottom – by the γ_{min} minimum number of wire layers from the same list. Limitations on the number of elements are imposed on the choice of the functional volume of the IC, taking into account the influencing factors – on top -N_{max}, and from the bottom - N_{min} (Fig.3).

To determine the experimental values of the γ and K indices as well as the PSR, let us analyze the behavior of these indicators (or their constancy curves) in the first quadrant of the coordinate system $\gamma(N)$.

From Fig.1 b, it can be seen that the $K = const$ constancy curve represents a growing dependence $\gamma(N)$. At that, the lower the constancy curve, the greater the value of the filling density coefficient. It is not difficult to be convinced of this by comparing the points located on two different constancy curves of K having the same abscissa. The point on the upper curve will correspond to a larger number of wire layers of the IC platform, than the point on the lower curve, which, in case of the same N number of displacement points of the elements on the integrated circuit platform, will ensure a more complete filling of the mounting area. Thus, the maximum value of K in the rectangle ABCD will be at the point D.

The computer analysis of expression (1) showed that the constancy curve of γ is a decreasing dependence of γ on K $[\gamma(K)]$ (Fig.1 a). At that, with the increase of K, the decrease of γ gradually slows down, and starting from some moment, the constancy curve of N practically turns into a path parallel to the axis K.

The four constancy curves $N = N_1, N = N_2, N = N_3, N = N_4$ are shown in Fig. 1 a.

By the similarity of the judgments obtained when comparing the two constancy curves of the parameter K, it can also be concluded: the lower the N constancy curve, the fewer the number of the structure elements it corresponds to. It follows that the minimum number of elements in the rectangle ABCD will be at point A. To determine the PSR, it is necessary to construct the $N = N_{min}$ and $K = K_{max}$ constancy curves, portioning as permissible solutions for each indicator the range below the extreme constancy curve.

The possible solutions to the problem depend on the resulting limiting constancy curves and the relative position or location of the rectangle ABCD [9, 10].

1. Let us consider all possible solutions when there is only one optimal solution by two indicators.

2. We will combine all the options, the solution of which requires the use of a compromise scheme.

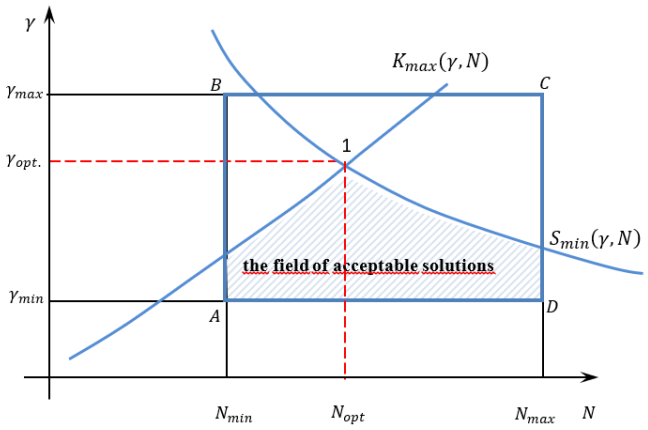

Fig. 3. Intersection of the curves of the $S(\gamma,N)$ surface of the mounting field and the density coefficient of the wires of the wire layer $K(\gamma,N)$ (constancy curves) in the field of acceptable solutions ABCD.

First of all, this class includes all cases when the constancy curves $S_{min}(\gamma,N)$ and $K_{max}(\gamma,N)$ intersect inside the rectangle ABCD. In this case, at the intersection point $1(N_{opt},\gamma_{opt})$ (Fig 3), by the selection of the N,γ parameters, the optimal values of two indicators can be ensured in the structure.

When considering other cases, the options for which the curve $S=S_{min}$ passes below point A or the curve $K=K_{max}$ passes below point D should not be considered. In this case, there is no optimal solution, and PSR does not exist.

When considering various options, it should be borne in mind that the only optimal solution for two indicators exists when the curve S_{min} runs down from point B and goes up above point A. Fig. 3 shows a possible variant when there are two curves S_{min} and K_{max} for two indicators (the optimal intersects at the point $1(\gamma_{opt},N_{opt})$) [9,10].

III. The Usage of "Synthese" Software Package

Using the "Synthese" software package, the best ratio between the number of wire layers and the number of elements of the mounting field of a printed circuit board or integrated circuit is determined, according to the minimum area of the mounting field and the maximum fill factor. After launching the "Synthese" software package, the studied field of a printed circuit board or integrated circuit is selected in the "Synthese" window (Fig. 4), after which the values provided for the necessary data are entered. Here, it is necessary to take into account that we have various technological opportunities, which are expressed by $d_{min},a,b,$ and $\boldsymbol{N}$ values [1-10].

The number of the MPC or IC platform wire layer is limited by the maximum value γ_{max} and by the minimum value γ_{min} (the number from the current list). The number of element limitations is imposed on the choice of the functional volume of the printed circuit board or integrated circuit, taking into account the influencing factors – maximum N_{max}, and minimum N_{min} (Fig.4,5). This area is the (γ,N) field in the Pareto range [9] according to the area $S_{min}(\gamma,N)$ of the printed circuit board or integrated circuit platform and the density coefficient $K_{max}(\gamma,N)$ of the wire layers in the mounting field (Fig. 4,5).

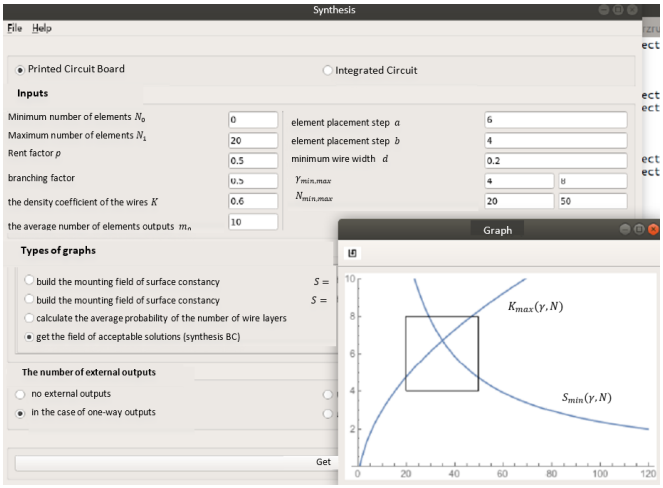

Fig. 4 The intersection of the constancy curves of the minimum area of the PCB mounting field and the layer wire density coefficient within the permissible solutions range
$\gamma_{min}=4,\gamma_{max}=8,N_{min}=20,N_{max}=50$

From the "Graph types" field, the field for constructing the permissible solution range (synthesis BC)" is selected, and by the button "Construct", the graphs of the selected data are plotted (Fig.4, 5).

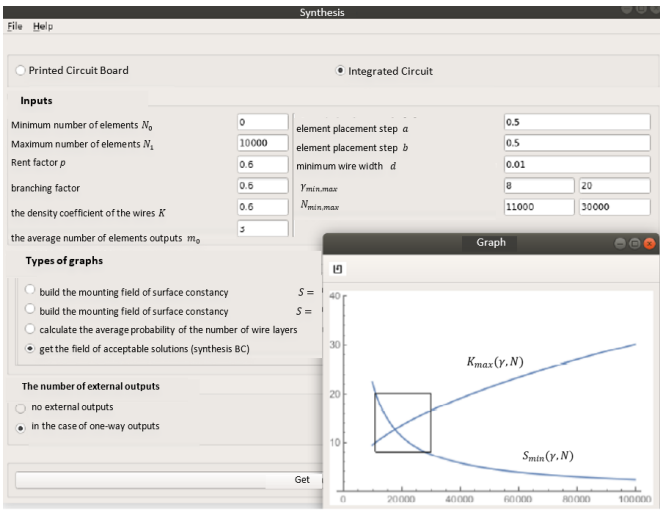

Fig.5. Intersection of the constancy curves of the minimum area of the integrated circuit mounting field and the wire density coefficient within the permissible solutions' range
$\gamma_{min}=8,\gamma_{max}=20,N_{min}=11000,N_{max}=30000$.

When the constancy curves $S_{min}(\gamma,N)$ and $K_{max}(\gamma,N)$ intersect in the Pareto range, then at the intersection point N_{opt},γ_{opt} (Fig. 4,5), by choosing the N,γ parameters, it is possible to provide the optimal values of two indicators $S(\gamma,N)$ and $K(\gamma,N)$ in the intersection point of the constancy curves (Fig. 6).

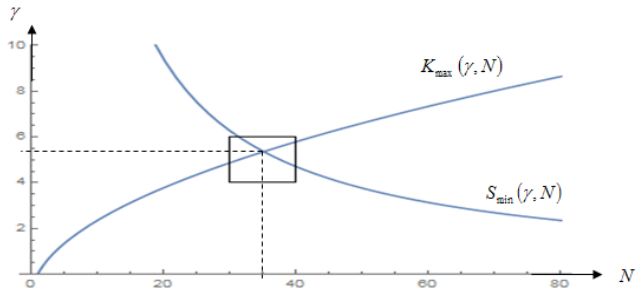

Fig.6. MPC platform of the constancy curves of the wire density coefficient and the surface of the IC mounting field in the area (γ, N).

IV. Conclusion

A two-parameter model for evaluating the wire layers of an integrated circuit has been developed.

Using the analytical dependence of the structural parameters of the integrated circuit on the number of wire layers, the area of the mounting field, the number of elements, the density coefficient of the mounting field of the platform, and the constancy curves, a number of structural parameters of IC and MPC have been evaluated at the early stages of design. It is shown that after determining the Pareto range, the fair compromise method is the most expedient in the case of multi-criteria synthesis of IC structures.

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